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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,279	11/19/2003	Steven J. Koester	YOR920030533US1 (17110)	7401

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/717,279	KOESTER, STEVEN J.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *10-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-9 in the reply filed on 7/26/05 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "said substrate" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leitz et al. (US Pat. Pub. 2004/0075105 A1) in view of Fitzgerald (U. S. Pat. 6,555,839 B2).

Regarding claim 1, Leitz et al. discloses in Fig. 6 a semiconductor field effect transistor device that comprises a first layer of semiconductor material doped of a first dopant type; a source region and a drain region (696, 697, 698, 699) implanted with dopants of a second opposite type (depending on the CMOS device); a gate electrode (690, 692) separated from the first layer by a dielectric region (688, 689) and positioned between the source and drain electrodes; and the substrate having one or more dislocations or crystal defects that extend continuously from the source to the drain region (as disclosed in ¶[0024], ¶[0054]).

Leitz et al. discloses the claimed invention with the exception of having blocking impurity dopant materials that partially or fully occupy the dislocation defects, wherein the blocking impurity dopant materials substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the dislocation or crystal defect.

Fitzgerald discloses in Fig. 6 a semiconductor field effect transistor device that comprises a first layer of semiconductor material doped of a first dopant type; a source region (618) and a drain region (620) implanted with dopants of a second opposite type; a gate electrode separated from the first layer by a dielectric region, and positioned between the source and drain electrodes (as shown by item 642); the substrate having one or more dislocation or crystal defects; and blocking impurity dopant materials (670) that partially or fully occupy the dislocation defects, wherein the blocking impurity dopant materials substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the dislocation or crystal defect (as shown in Figs 5C to

5H, and as taught in col. 5, lines 16-30) wherein blocking impurity dopant materials are used for the disclosed intended purpose of providing enhanced performance with a low power delay.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have blocking impurity dopant materials that substantially inhibit diffusion of the implanted source and drain dopants from diffusing along the dislocation or crystal defect (as shown in Figs 5C to 5H, and as taught in col. 5, lines 16-30 of Fitzgerald) wherein blocking impurity dopant materials are used by Fitzgerald for the disclosed intended purpose of providing enhanced performance with a low power delay.

Regarding claim 2, Leitz et al. discloses that the first layer of semiconductor material comprises silicon, silicon germanium, or germanium, as disclosed in ¶[0055].

Regarding claim 3, Leitz et al. discloses in Fig. 6 that the first layer of semiconductor material comprises a multi-layer structure comprising silicon and silicon germanium.

Regarding claim 4, Leitz et al. discloses in ¶{0062] that the first layer of semiconductor material comprises a SiGe relaxed substrate.

Regarding claims 5, and 6, Leitz et al. as modified by Fitzgerald discloses that the source and drain dopants comprise P, As, Sb, B, or In (as discloses in col. 4, ll. 15-30 and that the blocking impurity (taught as the buried channel) comprises In or Sb (as disclosed in col. 4, ll. 15-30).

7. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leitz et al. in view of Fitzgerald as applied to claims 1-6 above, and further in view of Ng et al. (U. S. Pat. 5,134,447).

Regarding claims 7, 8, and 9, Leitz et al., as modified by Fitzgerald, discloses the claimed invention with the exception of the blocking impurity comprising a neutral type impurity or a group IV impurity.

Ng et al. discloses a semiconductor field effect transistor that comprises a neutral impurity that includes germanium, carbon, tin, silicon, indium and lead, and wherein the dopants are taught for the disclosed intended purpose of increasing the operating lifetime of the device by preventing the formation of hot charger carriers at or near the drain thus inhibiting the diffusion of the implanted source and drain dopants along the substrate, as disclosed in col. 2, lines 20-52.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either of germanium, carbon, tin, silicon, indium and lead for the disclosed intended purpose of increasing the operating lifetime of the device by preventing the formation of hot charger carriers at or near the drain thus inhibiting the diffusion of the implanted source and drain dopants along the substrate, as disclosed in col. 2, lines 20-52.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814